UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,051	02/17/2004	Edward Flaherty	ALT-195 CON (A612 C1)	8388

36981 7590 01/03/2007

FISH & NEAVE IP GROUP
ROPES & GRAY LLP
1251 AVENUE OF THE AMERICAS FL C3
NEW YORK, NY 10020-1105

EXAMINER	
LEVIN, NAUM B	
ART UNIT	**PAPER NUMBER**
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/781,051	FLAHERTY ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *6-8 and 26-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9-25 and 35-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/781,051, Response to Election/Restriction filed on 10/16/2006, and Amendment filed on 07/19/2006. Applicants have elected claims 1-5, 9-25, and 35-40 (Group 1) without traverse. Independent claims 9, 17 and 35 have been amended and include additional limitations. Claims 6-8, and 26-34 have been withdrawn from consideration. Claims 1-5, 9-25, and 35-40 remain pending in the application.

2. The Examiner finds Applicant's arguments on the application Narasimhan as none persuasive. Narasimhan reference reads on the claims 1-5, 9-25, and 35-40 as presently written.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 9-25, and 35-40 are rejected under 35 U.S.C. 102(e) as being unpatentable by Narasimhan et al. (US Patent 6,446,192).

3. As to claims 1, 9, 17, and 35 Narasimhan discloses:

(1) A method of configuring an integrated circuit chip that includes programmable logic circuitry, said method comprising (Abstract):

programming said programmable logic circuitry to function as communications port circuitry (integrated circuit chip 36 that provides a direct link between the device control circuitry 38 and the network 32 – col.5, ll.12-14; the network interface chip 36 has the ability to communicate with sophisticated devices through standard parallel and serial interfaces, as well as the ability to communicate with simple devices through a programmable parallel interface - col.5, ll.25-29; A single self-contained and autonomous module for directly interfacing device control circuitry of a device to a client machine via a computer network, wherein ... device interface comprises ... a programmable input/output port- claims 1-5) (col.4, ll.65-67; col.5, ll.1-31; col.9, ll.21-39; col.15, ll.62-64; col.16, ll.5-15; claims 1-5);

establishing with said programmed programmable logic circuitry a connection between the said integrated circuit chip and an off-chip source of data for use in reprogramming said programmable logic circuitry (integrated circuit chip 36 that provides a direct link between the device control circuitry 38 and the network 32 – col.5, ll.12-14; the network interface chip 36 has the ability to communicate with sophisticated devices through standard parallel and serial interfaces, as well as the ability to communicate with simple devices through a programmable parallel interface - col.5, ll.25-29) (col.4, ll.37-54; col.4, ll.65-67; col.5, ll.1-31; col.6, ll.30-58);

transferring data from said off-chip source to said integrated circuit chip using said connection (integrated circuit chip 36 that provides a direct link between the device control circuitry 38 and the network 32 – col.5, ll.12-14; Standard TCP/IP provides the transport and network layers for passing data between the equipment 34 and the

remote client 30-col.6, ll.35-36) (col.5, ll.12-31; col.6, ll.30-46; col.12, ll.40-67; col.13, ll.1-3); and

using transferred data to reprogram said programmable logic circuitry to function as other ("IC 10 may also be used as an arbiter for arbitrating access to a shared resource in system 302" – Applicants Specification, page 18, ll.9-11) than communications port circuitry (As is evident from FIG. 2, the functionality of the chip is provided by a versatile collection of layered protocols – col.7, ll.49-50; a Security layer that provides standard security functionality, e.g., implemented as a secure sockets layer (SSL) or transport layer security (TLS)- col.7, ll.57-59; The preferred embodiment of the network interface chip provides security through login authentication ... Upon connection, the user is prompted for a password. If the password is not correct, the connection will be refused – col.9, ll.52-58) (col.7, ll. 31-67; col.9, ll. 50-60);

(9) An integrated circuit chip comprising:

programmable logic circuitry (col.4, ll.65-67; col.5, ll.1-31; col.9, ll.21-39; col.15, ll.62-64; col.16, ll.5-15; claims 1-5);

processor circuitry operative to program said programmable logic circuitry (The TCP/IP processor 66 handles header processing for the MAC, network (IP), and transport (TCP) layers. It also implements the transport layer functions such as packet re-assembly, re-transmit requests for dropped packets, and acknowledgement of received packets. The TCP/IP processor 66 guarantees that all network data is reliably transmitted and received – col.15, ll.54-60) (col.15, ll.40-67; col.16, ll.1-5); and

Ethernet media access controller (MAC) circuitry operative to establish a connection between said chip and an off-chip source of data, said Ethernet MAC circuitry coupled to said processor circuitry (A media access control (MAC) block 62 appropriately controls access to the physical network. Each type of network (RF, Ethernet, optical, etc.) requires a unique MAC functionality for that network type. Ethernet is the most common media in current use- col.15, ll.40-48),
said Ethernet MAC circuitry being operative to establish a connection between said integrated circuit chip and an off-chip source of a data so that said data from said off-chip source can be brought into said integrated circuit chip via said connection, after which said Ethernet MAC circuitry is operative to sever said connection, said processor circuitry being operative to program said programmable logic with said data brought into said integrated circuit chip via said connection for operation of said integrated circuit chip after said connection has been severed (The preferred embodiment of the network interface chip (36) provides security through login authentication ... Upon connection, the user is prompted for a password. If the password is not correct, the connection will be refused – col.9, ll.52-58) (col.3, ll.30-33; col.4, ll.65-67; col.5, ll.11-16; col.6, ll.53-55; col.9, ll.50-60; col.15, ll.40-55);

(17) An integrated circuit chip comprising:

programmable logic circuitry operative to be selectively programmed as communications port circuitry (col.4, ll.65-67; col.5, ll.1-31; col.9, ll.21-39; col.15, ll.62-64; col.16, ll.5-15; claims 1-5);

processor circuitry operative to program said programmable logic circuitry (col.15, ll.40-67; col.16, ll.1-5);

memory circuitry (Fig. 12: positions 68, 70, 74, 86);

Ethernet media access controller (MAC) circuitry operative to establish a connection between said chip and an off-chip source of data to bring said data for programming the programmable logic circuitry into the integrated circuit chip from the off-chip source via the connection, after which the Ethernet MAC circuitry severs the connection (The preferred embodiment of the network interface chip (36) provides security through login authentication ... Upon connection, the user is prompted for a password. If the password is not correct, the connection will be refused – col.9, ll.52-58) (col.3, ll.30-33; col.4, ll.65-67; col.5, ll.11-16; col.6, ll.53-55; col.9, ll.50-60; col.15, ll.40-55); and

interconnection bus circuitry coupled to said programmable logic circuitry, processor circuitry, memory circuitry, and Ethernet MAC circuitry (col.15, ll.36-67; col.16, ll.1-22, Fig. 12, Abstract);

(35) An integrated circuit chip comprising:

programmable logic circuitry operative to be selectively programmed as Ethernet media access controller (MAC) circuitry for establishing a connection between said integrated circuit chip and an off-chip source of a data to bring said data for further programming the programmable logic circuitry into the integrated circuit chip from the off-chip source via the connection, after which the programmable logic circuitry severs the connection (The preferred embodiment of the network interface chip (36) provides

security through login authentication ... Upon connection, the user is prompted for a password. If the password is not correct, the connection will be refused – col.9, ll.52-58); (col.3, ll.30-33; col.4, ll.65-67; col.5, ll.11-16; col.6, ll.53-55; col.9, ll.50-60; col.15, ll.40-67; col.16, ll.1-14);

processing circuitry operative to program said programmable logic circuitry (col.15, ll.40-67; col.16, ll.1-5);

receiver/transmitter circuitry (col.15, ll.49-52); and

interconnection bus circuitry coupled to said programmable logic circuitry, processing circuitry, and receiver/transmitter circuitry (col.15, ll.36-67; col.16, ll.1-22, Fig. 12, Abstract).

4. As to claims 2-5, 10-16, 18-25 and 36-40 Narasimhan recites:

(2) The method, wherein said transferring data to a memory on said integrated circuit chip uses said connection (col.15, ll.36-67; col.16, ll.1-22, Fig. 12, Abstract);

(3), (13), (14), (22), (23) The method/IC, wherein said programming comprises programming to function as Ethernet media access controller (MAC) circuitry (col.3, ll.30-33; col.4, ll.65-67; col.5, ll.11-16; col.6, ll.53-55; col.15, ll.40-55);

(4), (5) The method further comprising before said programming establishing a first connection between said integrated circuit chip and a first off-chip source of data (col.4, ll.37-54; col.6, ll.30-58; col.12, ll.40-67; col.13, ll.1-3col.15, ll.49-52);

(10), (19) The integrated circuit chip, wherein said processor circuitry is microprocessor circuitry (col.5, ll.20-23);

(11) The integrated circuit chip, wherein said programmable logic circuitry is reprogrammable (col.2, ll. 40-67; col.16, ll. 23-40);

(12), (21), (36), (37), (38) An end-user system comprising a circuit board comprising: a processor; a memory; 1/0 circuitry (Abstract; Fig.3- client hardware);

(15), (16), (18), (24), (25), (39), (40) The end-user system, wherein said end-user system comprises a data processing system (Abstract);

(20) The integrated circuit, wherein said memory circuitry is random access memory (RAM) (col.15, ll.62-64).

REMARKS

5. Mostly Applicant argues: "Claim 1 says that programmable logic circuitry on the chip is first used as the port through which a connection is made. Reprogramming data is brought into the chip via that port. Then that reprogramming data is used to reprogram the programmable logic circuitry to give that circuitry a function other than a communications port function. This is not shown in the '192 patent."

Narasimhan, for example, teaches: "integrated circuit chip 36 that provides a direct link between the device control circuitry 38 and the network 32 – col.5, ll.12-14; the network interface chip 36 has the ability to communicate with sophisticated devices through standard parallel and serial interfaces, as well as the ability to communicate with simple devices through a programmable parallel interface - col.5, ll.25-29; A single self-contained and autonomous module for directly interfacing device control circuitry of a device to a client machine via a computer network, wherein ... device interface comprises ... a programmable input/output port- claims 1-5". These examples

correspond to "programmable logic circuitry on the chip is first used as the port" in Applicants remarks.

Next Narasimhan, for example, recites: "The preferred embodiment of the network interface chip can operate in one of two fundamental modes: Data Pass Through: network interface chip passes data transparently between the device and the Internet. Network Peripheral: The device interfaces to the network interface chip through an API, allowing the device access to more functionality and services – col.11, ll.3-9". This sentence corresponds to "Reprogramming data is brought into the chip via that port" in Applicants remarks.

Next Narasimhan, for example, discloses: " As is evident from FIG. 2, the functionality of the chip is provided by a versatile collection of layered protocols – col.7, ll.49-50; a Security layer that provides standard security functionality, e.g., implemented as a secure sockets layer (SSL) or transport layer security (TLS)- col.7, ll.57-59; The preferred embodiment of the network interface chip provides security through login authentication ... Upon connection, the user is prompted for a password. If the password is not correct, the connection will be refused – col.9, ll.52-58". These examples correspond to "Then that reprogramming data is used to reprogram the programmable logic circuitry to give that circuitry a function other than a communications port function." In other words "security functionality" is the function other than the communication function.

As to claims 9, 17 and 35 Applicants provided the same arguments as for claim1, so Examiner has the same explanations as above.

6. The Examiner finds Applicant's arguments on the application Narasimhan as none persuasive.

7. Accordingly, **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

N L

Thuan
THUAN DO
Primary examiner.
12/21/06